52

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/689,533	10/12/2000	Motoshi Ito	YAMAP0741US	9029

7590 11/05/2003

Neil A DuChez
Renner Otto Boisselle & Sklar LLP
1621 Euclid Avenue
19th Floor
Cleveland, OH 44115

EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 11/05/2003

8

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/689,533	Applicant(s) ITO ET AL.	
	Examiner Zhuo H. Li	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21,23-25 and 27-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21,23-25 and 27-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. This Office action is in response to the amendment filed 10/3/2003(paper no. 7).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-6, 8-21, 23-25 and 27-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis (US PAT. 5,963,970) in view of Assar et al. (US PAT. 5,479,638 hereinafter Assar).

Regarding claim 1, Davis discloses an apparatus for keeping track of erase cycles performed on a plurality of storage blocks in a flash memory comprising the non-volatile memory (10, figure 1), at least one WORD (20, figure 1) of a non-volatile memory, each WORD including a plurality of bits (col. 2 lines 56-63) and information can be erase from the non-volatile memory in a unit of sector, each sector including a plurality of WORDs, and wherein the non-volatile memory comprises an information storage area including at least one WORD in a first sector of the non-volatile memory (col. 4 lines 10-27), and a microprocessor (105, figure 2) for writing pieces of information in a predetermined order in the WORDs of the information storage area (col. 3 line 31 through col. 4 line 9). Davis differs from the claimed invention in not specifically teaching for reading out a last piece of information which has been written in the at least one WORD of the information storage area within a predetermined permitted update count. However, Assar teaches an algorithm for leveling erase cycles amongst all the blocks within a mass storage device comprising a counter for count the number of times each block has been erased and reprogrammed, so that a last piece of information which has been written in a one block of the information storage area within a predetermined permitted update count is read out (col. 6 line 56 through col. 9 line 4), thereby extending the life of the entire mass storage. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Davis in reading out a last piece of information which has been written in the at least one WORD of the information storage area within a predetermined permitted update count, as per teaching of Assar, because it extends the life of the entire mass storage.

Regarding claim 2, Assar discloses to erase all of the bits of all of the WORDs in the sector including the information storage area (col. 7 lines 51-56).

Regarding claim 3, Davis discloses to set all the bits of all of the WORDs in each sector to "1" (figure 4 and col. 4 line 42 through col. 5 line 52).

Regarding claim 4, Davis teaches to provide the information storage area in a same sector as an initialization operation program which is a first program to be executed after a reset (figure 3 and col. 4 lines 10-41).

Regarding claim 5, Davis discloses the predetermined order is an ascending order ot the address of the WORDs (figure 1).

Regarding claim 6, Assar discloses an upper limit value if the predetermined permitted update count being determined based on the number of WORDs in the information storage area (col. 7 lines 13-30).

Regarding claims 8-9, Davis teaches to set to a CLEAR state for an erase operation (col. 4 line 66 through col. 5 line 20) so that it recognizes to write at least one write one or more of the plurality of bit in the at least one WORDs from "1" to "0", and the WORDs in the information storage area being searched through in the predetermined order (figure 1-3 and col.4 lines 13-15). Although Davis does not specifically teaching to read out as the last piece of information, which has been written in the information storage area within the predetermined permitted update count, a last hit WORD found in a search through the information storage area for WORDs in which at least one bit is "0", Assar teaches an algorithm for leveling erase cycles amongst all the blocks within a mass storage device comprising a counter for count the number of times each block has been erased and reprogrammed, so that a last piece of information which

has been written in a one block of the information storage area within a predetermined permitted update count is read out including a last hit WORD found in a search through the information storage area for WORDs in which at least one bit is "0" (figure 6 and col. 6 line 56 through col. 9 line 4), thereby extending the life of the entire mass storage. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Davis in reading out a last piece of information which has been written in the at least one WORD of the information storage area within a predetermined permitted update count, as per teaching of Assar, because it extends the life of the entire mass storage.

Regarding claim 10, Assar teaches to store the number of times information has been written in the information storage area in an update count storage (abstract and col. 6 lines 56-60).

Regarding claim 11, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 12, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 13, Davis teaches the first sector including a first program to be executed by the microprocessor unit (figure 3 and col. 4 lines 10-41).

Regarding claim 14, the limitations of the claim are rejected as the same reasons set forth in claim 5.

Regarding claim 15, the limitations of the claim are rejected as the same reasons set forth in claim 6.

Regarding claim 16, the limitations of the claim are rejected as the same reasons set forth in claim 7.

Regarding claims 17-18, the limitations of the claim are rejected as the same reasons set forth in claims 8-9.

Regarding claim 19, the limitations of the claim are rejected as the same reasons set forth in claim 10.

Regarding claim 20, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 21, the limitations of the claim are rejected as the same reasons set forth in claim 1. In addition, Davis teaches to provide the information storage area in a same sector as an initialization operation program which is a first program to be executed after a reset (figure 3 and col. 4 lines 10-41).

Regarding claims 23-24, Assar teaches an information update count managing method wherein the contents usage count is read out as the number of remaining times or as the number of times the content can be used (col. 7 line 57 through col. 8 line 7).

Regarding claim 25, the limitations of the claim are rejected as the same reasons set forth in claim 1. In addition, Davis teaches the first sector of the non-volatile nmemory including a first program to be executed by the microprocessor unit (figure 2 and col. 3 line 59 through col. 4 line 9).

Regarding claim 27-28, the limitations of the claim are rejected as the same reasons set forth in claims 23-24.

Regarding claim 29, Regarding claim 1, Davis discloses an apparatus for keeping track of erase cycles performed on a plurality of storage blocks in a flash memory comprising the non-volatile memory (10, figure 1), at least one WORD (20, figure 1) of a non-volatile memory, each WORD including a plurality of bits (col. 2 lines 56-63) and information can be erase from the non-volatile memory in a unit of sector, each sector including a plurality of WORDs, and wherein the non-volatile memory comprises an information storage area including at least one WORD in a first sector of the non-volatile memory (col. 4 lines 10-27), and a microprocessor (105, figure 2) for writing pieces of information in a predetermined order in the WORDs of the information storage area (col. 3 line 31 through col. 4 line 9), wherein the non-volatile unit memory includes a boot area and a system area each including one or more sectors such that the boot area includes an information storage area including at least one WORD and a microprocessor unit initialization program for initializing the microprocessor unit (figure 3 and col. 3 line 59 through col. 4 line 41). Although Davis does not specifically teaching to read out as the last piece of information, which has been written in the information storage area within the predetermined permitted update count, a last hit WORD found in a search through the information storage area for WORDs in which at least one bit is "0", Assar teaches an algorithm for leveling erase cycles amongst all the blocks within a mass storage device comprising a counter for count the number of times each block has been erased and reprogrammed, so that a last piece of information which has been written in a one block of the information storage area within a predetermined permitted update count is read out including a last hit WORD found in a search through the information storage area for WORDs in which at least one bit is "0" (figure 6 and col. 6 line 56 through col. 9 line 4), thereby extending the life of the entire mass storage.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Davis in reading out a last piece of information which has been written in the at least one WORD of the information storage area within a predetermined permitted update count, as per teaching of Assar, because it extends the life of the entire mass storage.

Regarding claim 30, Davis teaches the memory having support softeware to control the setting within the information storage area (col. 3 line 64 through col. 4 line 3) so that the boot area obviously comprises a check program for checking contents of the information storage area.

Regarding claim 31, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 32, the boot area further comprises I/F control means for receiving a program to be stored in the system area from an upper control unit which is connected to the information update count managing apparatus (figure 3).

Regarding claim 33, Davis discloses flash memory update means (245, figure 3) for updating a program in the system area.

Regarding claim 34, Assar teaches the microprocessor unit executes the microprocessor unit initialization program, and then waits for reception from the upper control nit which is connected to the information update count managing apparatus immediately after the micro processor unit is reset (col. 6 line 56 through col. 7 line 30).

Regarding claim 35, Davis discloses the microprocessor unit calls a program in the boot area from a grogram in the system area (col. 5 line 53 through col. 6 line 6).

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Davis (US PAT. 5,963,970) in view of Assar et al. (US PAT. 5,479,638 hereinafter Assar) as applied to claims above, and further in view of Sawabe (US PAT. 6,122,434).

Regarding claim 7, the combination of Davis and Assar differs from the claimed invention in not specifically teaches the information update count managing method wherein the pieces of information include regional information which is used for controlling a region where a content can be reproduced. However, Sawabe an information recording medium including regional information, which is used for controlling a region where content can be reproduced (col. 2 line 9 through col. 4 line 35). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Davis and Assar in having the pieces of information include regional information which is used for controlling a region where a content can be reproduced, as per teaching of Sawabe, because it makes user friendly by reproducing an identical disk in different ways according to predetermined levels which are set differently in various countries.

Response to Arguments

5. Applicant's arguments with respect to claims 1-1-21, 23-25 and 27-35 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 746-7239

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 703-305-3846. The examiner can normally be reached on Tuesday to Friday from 9:30 a.m. to 7:00 p.m. The examiner can also be reached on alternate Monday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Zhuo H. Li

Art Unit 2186

Mano Padmanabhan
11/3/03

Mano PADMANABHAN
SUPERVISORY PATENT EXAMINER
TC 2100